WASHINGTON STATE UNIVERSITY
VANCOUVER
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School of Engineering and Computer Science

ECE 214: Design of Logic Circuits
Master Syllabus

Catalog Data:	**ECE 214: Design of Logic Circuits**; 3 credits (2-3) Design and application of combinational logic circuits with exposure to modern methods and design tools; introduction to sequential logic circuits. Typically offered in Spring.
Class Schedule:	Two lecture hours per week, for one semester.
Laboratory Schedule:	One 3-hour lab session per week, for one semester.
Prerequisites by Course:	ECE 101; MATH 106, or a minimum ALEKS math placement score of 80%.
Prerequisites by Topic:	1. Familiarity with logic concepts. 2. Basic understanding and experience in using electrical engineering lab equipment such as oscilloscopes, function generators, power supplies and breadboard level circuit wiring.
Required Text(s):	Morris Mano and Michael D. Ciletti , *Digital Design, 5th Edition*, Prentice Hall, 2013
Reference(s):	R. H. Katz, *Contemporary Logic Design, 2nd Edition*, Prentice Hall, 2004
Course Coordinator:	Dr. John Lynch
Course Objectives:	1. Design, analyze and implement combinational and sequential logic circuits using basic logic gates. 2. Perform minimization of logic expressions using Karnaugh maps and canonical standard forms. 3. Design and analyze logic circuits using or implementing arithmetic operations, multiplexers, encoders, simple latches and flip-flops. 4. Understand the design, optimization and implementation of finite state machines.
Topics Covered:	1. Overview and history of digital technology 2. Number systems, binary arithmetic and encoding 3. Binary state terminology, CMOS terminology and symbology, basic logic functions, Boolean algebra, digital logic gates 4. CMOS transistor level gate implementation and an overview of integrated circuit design 5. Gate level logic minimization and use of minimization tools or techniques 6. Design, analysis and application of combinational logic: multiplexers, decoders, encoders, comparators, parity circuits, and shifters 7. Design and application of basic arithmetic circuits such as adders, and subtractors 8. Introduction to sequential logic machines-latches, flip-flops, registers, and counters 9. Application of programmable logic devices (ROMs, PLAs, PALs) to combinational logic design 10. Finite state machines (Mealy & Moore types) and state minimization 11. Introduction to timing defects (hazards) and races in combinational logic circuits

<table>
<tr><td colspan="2">Lab Experiments and Activities:</td><td colspan="3">Lecture sessions converted into laboratory sessions as needed for demonstrations and hands-on activities. These activities are translated into -but not limited to- the following experiments:

1. OR, AND, and inverter gates
2. Two's complement addition and subtraction
3. Boolean theorems
4. 3-variable Karnaugh map logic simplification
5. 4-variable Karnaugh map for 7-segment display
6. Cost optimization
7. Display using a decoder, and PWM using a comparator
8. Asynchronous SR latches
9. Flip-flops and shift registers
10. Modulo counters
11. State machine analysis, and linear feedback shift registers
12. Finite state machine with datapath using a counter and multiplexers.</td></tr>
<tr><td rowspan="3">Course Outcomes:</td><td colspan="4">Students will be able to</td></tr>
<tr><td>Assessed for Student Outcomes</td><td colspan="3">3.a. Present findings of experiments in formal report format(s) including figures, tables, graphs, citations.
4.a. Evaluate economic tradeoffs in digital systems by using timing constraints and logic minimization.
6.b. Utilize basic electrical engineering lab equipment such as oscilloscopes, function generators, power supplies, multimeters, LEDs, seven-segment displays and their interface to digital ICs for experiments to collect data.</td></tr>
<tr><td>Other</td><td colspan="3">1.c. Use appropriate models, such as Boolean algebra and Karnaugh maps, to formulate solutions for digital logic circuits
6.d. Draw conclusions by evaluating experimental results with respect to system level design specifications.
7.a. Able to use resources such as data sheets for digital ICs, manuals for lab equipment and tutorials for CAD tools to learn new material not taught in class.</td></tr>
<tr><td colspan="2">Relationship of Course to Program:</td><td colspan="3">Meets: Educational Objectives <u>1, 2, 3, 4</u>
Student Outcomes <u>3, 4, 6, 7</u></td></tr>
<tr><td colspan="2">Prepared by:</td><td>Dr. John Lynch</td><td>Date:</td><td>March 2, 2018; 3/21/18 (mb)
Reviewed 02/12, revised 10/2015, revised 09/2017 revised 10/08/18 revised 5/21/24</td></tr>
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