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**School of Engineering and Computer Science**

# ECE 366: Introduction to VLSI Design
# Master Syllabus

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| ***Catalog Data:*** | **ECE 366: Introduction to VLSI Design**; 3 credits (2-3)<br>CMOS devices and deep-submicron fabrication technology; interconnect modeling, power and clock distribution, area, power, and speed optimization. Typically offered in Spring. |
| ***Class Schedule:*** | Two lecture hours per week, for one semester. |
| ***Laboratory Schedule:*** | One 3-hour lab session per week, for one semester. |
| ***Prerequisites by Course:*** | ECE 214; ECE 349 |
| ***Prerequisites by Topic:*** | 1. Familiarity with logic concepts, digital circuits and modern CAD tools.<br>2. Basic experience in schematic level design entry and simulation of electronic circuits using SPICE.<br>3. Basic understanding and experience in designing, analyzing and optimizing digital systems (combinational/sequential) employing logic gates.<br>4. Basic knowledge of semiconductor device electronics. |
| ***Typical Text(s):*** | J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits, 2nd Edition*, Prentice-Hall, 2003. |
| ***Typical Reference(s):*** | N.H.E. Weste, and K. Eshraghian, *Principles of CMOS VLSI Design, 2nd Edition*, Addison Wesley, 2004.<br>M. J. S. Smith, *Application-Specific Integrated Circuits*, Addison-Wesley, 1997.<br>R. J. Baker, *CMOS Circuit Design, Layout, and Simulation, 2nd Edition*, Wiley-IEEE, 2007. |
| ***Course Coordinator:*** | Dr. John Lynch |
| ***Course Objectives:*** | 1. Learn to design and implement state-of-the-art digital Very Large Scale Integrated (VLSI) chips using CMOS technology.<br>2. Utilize workstation-based modern CAD tools to complete VLSI projects and to build industry standard design libraries.<br>3. Introduce the principles of digital integrated circuit design, layout, optimization and verification at transistor, gate and system levels. |
| ***Topics Covered:*** | 1. Overview of digital integrated circuits<br>2. Manufacturing/Fabrication Processes<br>3. CMOS Integrated Circuits<br>• Design Rules<br>• Trends in Process Technology<br>4. MOSFET transistors<br>5. CMOS Inverter<br>6. Design of Combinational Gates<br>• Static CMOS<br>• Dynamic CMOS<br>7. Design of Sequential Logic Gates<br>• Latches<br>• Registers<br>8. Cell-based Design Methodology |

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| | | 9. Timing Issues in Digital Circuits<br>10. Layout Techniques, full-custom design<br>11. Circuit Simulation<br>• Interconnect (resistance, capacitance, inductance)<br>• Wire models<br>12. Design for Testability<br>13. Packaging and Testing | | |
| ***Lab Experiments and Activities:*** | | Lecture sessions converted into laboratory sessions as needed for demonstrations and hands-on activities. These activities are translated into -but not limited to- the following experiments:<br><br>1. Tutorial on using Cadence Design Environment<br>2. Inverter Schematic, Symbol<br>3. Inverter Simulation: Transient, DC w/parametric, Voltage transfer characteristics<br>4. Inverter Layout, DRC, Extraction, and LVS<br>5. NAND gate Schematic, Test Bench, Simulation, and Layout<br>6. Cell Interconnection, Routing Techniques<br>7. Back Annotation, simulation of extracted view, post-layout characterization<br>8. Dynamic Circuits using Domino Logic | | |
| ***Course Outcomes:*** | Students will be able to: | | | |
| | ***Assessed for Student Outcomes*** | 1-d. Apply probability and statistics in analyzing die yield, fault models, and testing of VLSI chips.<br>2-b. Apply design process to satisfy project requirements for VLSI devices and systems.<br>6-a. Identify constraints, assumptions, and models for VLSI circuit experiments. | | |
| | ***Other*** | 2-a. Define engineering problems from specified needs for VLSI devices.<br>3-a. Produce lab reports using appropriate formats and grammar with discipline-specific conventions.<br>6-b. Use appropriate simulation and modeling techniques for VLSI circuit experiments.<br>6-c. Conduct analysis and interpretation of the data.<br>6-d. Draw conclusions by evaluating experimental results. | | |
| ***Relationship of Course to Program:*** | | Meets: Educational Objectives 1, 2, 4<br>Student Outcomes 1, 2, 3, 6 | | |
| ***Prepared by:*** | | Dr. John Lynch | Date: | Revised 3/2018, 3/21/18 (mb); December 30, 2009 reviewed 01/12 Reviewed 02/12, 11/02/18 JL/mb |