WASHINGTON STATE UNIVERSITY
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School of Engineering and Computer Science

ECE 324: Digital Systems Design
Master Syllabus

Catalog Data:	**ECE 324: Digital Systems Design**; 3 credits (2-3) Implementation of datapaths and controllers, use of hardware description languages and automated synthesis tools, field programmable gate arrays and simulation; integrated circuit layout. Typically offered in Spring.
Class Schedule:	Two lecture hours per week, for one semester.
Laboratory Schedule:	One 3-hour lab session per week, for one semester.
Prerequisites by Course:	ECE 214
Prerequisites by Topic:	1. Familiarity with logic concepts and basic digital circuits. 2. Basic understanding and experience in designing, analyzing and optimizing digital systems (combinational/sequential) employing logic gates.
Typical Text(s):	Pong P. Chu, *FPGA Prototyping By Verilog Examples: Xilinx Spartan-3 Version*, Wiley, 2008
Typical Reference(s):	Michael D. Ciletti , *Modeling, Synthesis and Rapid Prototyping with the Verilog HDL*, Prentice Hall, 1999
Course Coordinator:	Dr. John Lynch
Course Objectives:	1. Use hardware description languages to design and synthesize medium and large-scale logic blocks. 2. Realize designs on a Field Programmable Gate Array (FPGA) environment and testing designs in the laboratory.
Topics Covered:	1. Review of combinational and sequential logic circuits 2. Verilog HDL constructs Syntax, Data Types, Primitives Module Concept Structural Modeling Behavioral Modeling Advanced Modeling Techniques RTL System Design Methodology 3. Verification Simulation Functional Verification Testbench Design Dynamic/Static Timing Analysis 4. Synthesis tools Design Environment, Flow, Constraints Logic Synthesis FPGA Design Flow 5. Designing datapaths and associated control logic 6. FPGA based design/verification/synthesis flow and implementation

Lab Experiments and Activities:		Lecture sessions converted into laboratory sessions as needed for demonstrations and hands-on activities. These activities are translated into -but not limited to- the following experiments 1. Design entry, simulation, compilation in FPGA software suite 2. Synthesis, place/route, and device programming on FPGA development boards 3. Barrel Shifter 4. ALU 5. Counters 6. Synchronous Logic and Memory 7. FSM Implementation 8. VGA Controller 9. VGA Animation 10. Final Project		
Course Outcomes:	Students will be able to			
	Assessed for Student Outcomes	2-a. Define engineering problems from specified needs for digital systems including implementation on FPGAs using HDL programming. 2-d. Produce FPGA designs that meet specified needs. 3-b. Deliver well-organized, logical oral presentations accommodating audience interests and background, including good explanations when questioned. 5-a. Establish project goals, tasks and timeline, as a team. 5-b. Share responsibilities and information on project schedule and tasks with other members of the team. 5-c. Collaborate with individuals with diverse backgrounds, skills and perspectives. 7-b. Employ appropriate learning strategies such as communicating with an expert, using external resources, experimentation, simulation, etc.		
	Other	2-b. Apply design process to satisfy project requirements for digital systems including implementation on FPGAs using HDL programming. 3-a. Produce documents for various audiences using appropriate formats and grammar with discipline-specific conventions including citations. 7-a. Use resources effectively to learn new material not taught in class. 7-c. Apply new knowledge in designing FPGA solutions.		
Relationship of Course to Program:		Meets: Educational Objectives 1, 2, 3, 4 Student Outcomes 2, 3, 5, 7		
Prepared by:		Dr. John Lynch	Date:	Dec. 30, 2009 Revised 1/12 Reviewed 02/12, Revised 9/4/12, Revised 03/2018; 3/21/18 (mb)