Master Course Syllabus
School of Engineering and Computer Science
Washington State University Vancouver
CS 260
Computer Organization
3 Semester Hours
(3 lecture hours)

Catalog Description
Introduction to computer architecture, data representation, design and analysis of instruction sets, implementation of machine instructions, virtual memory and multiprocessing.

Prerequisite Courses
- CS 122 with a C or better
- CS 166 with a C or better

Prerequisite Topics
- Knowledge of an imperative programming language
- Experience designing and implementing programs using dynamic and self-referential data structures.

Measured Course Outcomes
Students taking this course will:
1. Analyze and design computing circuits at a variety of abstraction levels. (Contributes to 2-a)
2. Demonstrate an ability to design and implement software using the assembler and debugger for a RISC-style processor. (Contributes to Performance Criterion 6-d)

Required Textbooks
One of the following:
- *Digital Design and Computer Architecture*, David Harris and Sarah Harris
- *Computer Organization and Design, The Hardware/Software Interface*, David Patterson and John Hessessy.
- *Structured Computer Organization*, Andrew S. Tannenbaum.

Reference Material
None specified.

Major Topics Covered in the Course
1. Computer instructions and assembly language
2. Computer arithmetic and data representation
3. Logic design and semiconductor technology
4. CPU datapaths
5. Instruction set implementation and performance
6. Memory architecture and hierarchy

7. Input/Output and Interrupts
8. Parallelism and multiprocessing

Projects
Programming projects will include one or more assignments requiring students to design, implement and debug a program with multiple callable modules, in assembly language, using specific calling conventions and stack frame format.

CS2013
This course provides coverage of CS2013 knowledge areas. Values listed are minimum course hours dedicated to the topic, percentages indicate the fraction of CS2013 knowledge area topics covered (acceptable values are: <25%, 25-75%, >75%, or 100%).

Area	Tier 1	Tier 2	Elective
DS/Basic Logic	1 (<25%)		
AR/Digital Logic and Digital Systems		6 (25-75%)	
AR/Machine Level Representation of Data		5 (>75%)	
AR/Assembly Level Machine Organization		6 (>75%)	
AR/Memory System Organization and Architecture		5 (>75%)	
AR/Interfacing and Communication		2 (<25%)	
AR/Functional Organization			4 (25-75%)
AR/Multiprocessing and Alternative Architectures			1 (<25%)
OS/Memory Management	3 (100%)		1 (<25%)
AR/Performance Enhancements			1 (<25%)
PD/Parallel Architecture	2 (>75%)	1 (25-75%)	1 (<25%)

Design and Analysis
The instructor performs analyses of representative problems in class. Student assignments require the student to analyze problem requirements. A particular emphasis is made in analyzing the space and time tradeoffs of both multiple datapath architectures. Also, the cost/time tradeoffs involved in the design of instruction sets and memory cache architectures are analyzed.
Students are assigned logic or data-path design problems for which they are expected to arrive at designs which meet constraints while performing a specified function. Representative problems are solved in class by the instructor, textbook material and homework problems provide students with the skills and knowledge to be applied when developing their own designs.

Course Coordinator:	Paul Bonamy
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